

DGPS Receiver Hardware Description

Jim Bixby

bix@san.rr.com

November, 1998

Copyright Notice: The information in this document and in the zip archive are copyright Jim Bixby 1998. License is granted to freely use, reproduce or modify this material, for non-commercial purposes only. This information carries no warranty of any kind, including any implied warranty of fitness for any particular purpose.

Table of Contents

1. Introduction
2. ZIP Archive Files
3. Design Goals
4. Block Diagram
5. Active Antenna Preamp
6. RF Amp
7. Receiver
8. PLL Detector
9. Processor
10. PLL Design Information
11. Comments on Antennas
12. Comments on Design Modifications
13. Comments on Parts Cost and Selection
14. Initial Debugging and Tuning

List of Figures

- 5.1 Active Antenna Preamp Frequency Response
- 6.1 RF Amp Frequency Response
- 6.2 Combined Active Antenna Preamp and RF Amp Frequency Response
- 6.3 Combined Response, Two Coils per Amplifier
- 7.1 First IF Filter Frequency Response
- 7.2 Second IF Filter Frequency Response
- 9.1 LCD Display

1. Introduction

This document describes the hardware component of a differential DGPS beacon receiver. The receiver can receive DGPS beacon transmissions in the marine beacon band (285-325 kHz) and demodulate the transmission to extract the digital data stream with the DGPS information. A microprocessor takes that data, and outputs SC104-format digital data to a "DGPS-ready" GPS receiver at 4800 or 9600 baud. Receiver status and the decoded Station ID are displayed on a 16x2 LCD display.

2. ZIP Archive Files

The ZIP archive contains the following files:

Hardware.doc	This document
Software.doc	Software description
dgps.asm	Software source code file
dgps.hex	Software hex file
Block Diagram.wmf	Receiver block diagram
ActiveAntenna.wmf	Active Antenna Preamp schematic
RF Amp.wmf	RF Amplifier schematic
Receiver.wmf	Receiver schematic
PLL Detector.wmf	Schematic for FM demodulator
Processor.wmf	Schematic for the processor and freq. Synthesizer
Front Panel.wmf	Front panel schematic
RcvrBoard.gif	Annotated photo of the author's receiver breadboard
ActiveAntenna.gif	Annotated photo of the author's active antenna preamp
PartsList.xls	Excel spreadsheet of the parts lists
URL.txt	URLs to relevant spec sheets, application notes, and other information

The schematics are in Windows Metafile (.wmf) format. Word, PowerPoint, and most other Windows applications can open .wmf files.

3. Design Goals

The goals for this receiver were:

- High performance:
 - Low noise
 - High sensitivity
 - Excellent adjacent channel and image rejection
- Buildable from parts available to hobbyists
(All of the components can be purchased from Digikey or Newark)
- Parts cost of less than \$100 (somewhat exceeded this cost)

Specifications:

Power: 10-16vdc, 35 ma, plus LCD backlight current (50 ma)
Operation: Manual.
Receiver: 285-325 khz, in 1 khz steps, controlled by UP and DOWN
pushbutton switches
Receiver input noise: about 3 nv/root hz.
Sensitivity: better than 10 uv
Output: SC104 serial data, selectable to be 4800 or 9600 baud

Note: building this receiver is not for the inexperienced.

4. Block Diagram

Block Diagram.wmf contains the receiver block diagram. The receiver can use a loopstick antenna or a short vertical whip, and the input can be provided directly to the RF Amp block, or through an Active Antenna Preamp, which is almost identical in design to the RF Amp. Both are 3-pole filters with a small amount of gain, low input capacitance, low noise, and high input impedance.

After bandpass filtering and gain, the signal is fed to dual-conversion FM receiver, with the first IF frequency at 122 kHz and the second IF at 3 kHz. A very low frequency was chosen for the second IF to facilitate achieving a narrow bandpass filter for the second IF filter, and to make the FSK deviation of the input signal relatively larger compared to the carrier frequency, at the input to the FM demodulator to ease demodulation. The 1st local oscillator is synthesized, and the 2nd local oscillator is obtained by dividing down the processor clock.

The output of the receiver's limiter is fed to an FM demodulator which locks onto and demodulates the FSK signal and converts it to a digital signal. The demodulated digital data stream is then supplied to the PIC 16F84 processor, which

performs bit, word and frame synchronization, outputs data, and controls, monitors and displays receiver status on the LCD display.

5. Active Antenna Preamp

ActiveAntenna.wmf shows the schematic of the Active Antenna Preamp. The antenna input signal goes to a jfet-input cascode amplifier. The input noise is about 2-3 nv/root hz and input capacitance is about 3 pf. This preamp should be located right at the base of a whip antenna. The source impedance of an electrically short whip antenna (short compared to a wavelength) is equivalent to a low impedance source fed thru a series capacitor of about 10 pf per meter, so a voltage divider is formed between the antenna capacitance and the amplifier input capacitance. Thus, the longer (and larger in diameter) the whip, the larger the antenna capacitance, and thus the smaller is the signal loss due to the capacitive divider. In practice, a one-meter antenna should be fine for most uses. I selected a Radio Shack 8-foot whip for use on my boat.

The file ActiveAntenna.gif shows the completed antenna preamp. It is built on a small piece of vector board, and fits inside a housing made from 2" PCV pipe components. The preamp is held in place by a single 1/4-20 bolt which passes thru a right-angle brass plumbing fitting attached to the board, and out the top of the antenna housing. An antenna mount (Radio Shack 21-950) is screwed onto the bolt, and the mount provides a 3/8-24 threaded base for standard 3/8" whip antennas, such as a 102" fiberglass whip (Radio Shack 21-905) or a 39" stainless steel whip (Radio Shack 21-952). Large stainless steel washers are used above and below the top cap of the housing to increase strength.

The bottom cap of the antenna mount is a 3/4" female threaded adapter, which fits standard marine antenna mounts. The output cable is fed thru the bottom hole of the housing and thru the mast mount. After installation, RTV can be used to provide a weather seal.

The preamp is powered by 8vdc provided by the antenna cable from the receiver. The supply voltage is filtered by C106/C107, and supplied to the input cascode stage.

The filter in the preamp is a 3-pole design whose bandpass covers the marine beacon band. The nominal frequency response is shown in figure 5.1.

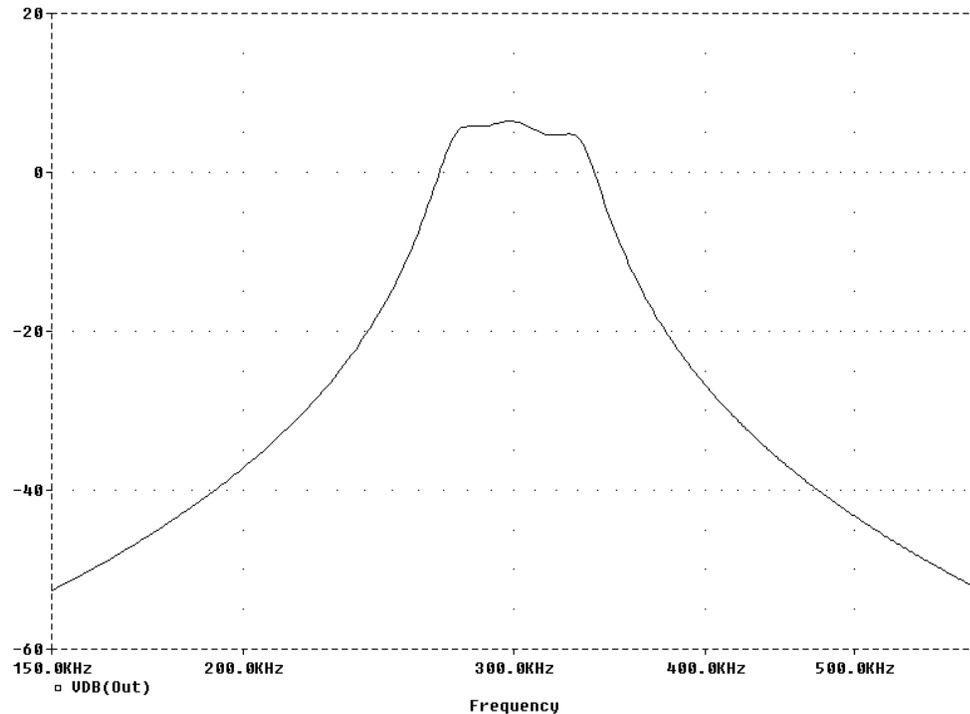


Figure 5.1
Active Antenna Preamp Frequency Response

Filter tuning for both the Active Antenna Preamp and the RF Amp (the designs are almost identical) is best done with a sweep generator, with the horizontal axis of an oscilloscope driven from the sweep output so that it represents frequency. Even better would be a spectrum analyzer with a tracking oscillator. Tune the filter for -3db points just outside of 285-325 khz, and a passband response which is reasonably flat.

6. RF Amp

RF Amp.wmf depicts the RF Amp, which very similar to the Active Antenna Preamp. The antenna can be connected directly to this amplifier, and the Active Antenna Preamp eliminated altogether, as long as there is no cable length between the antenna and the receiver.

Jumper W1 on the schematic allows for providing 8vdc power to the Active Antenna Preamp. L4 greatly reduces the input impedance, so leave this jumper out if you are not using the preamp.

Jumper W2, when installed, increases the RF Amp gain by about 6 db, and is provided for use on weak signals, when the antenna is connected directly to the receiver.

Figure 6.1 shows the RF Amp frequency response. The upper trace shows the response when the jumper for C3 is in place, and the lower trace shows the reduced gain when the jumper is not present. Figure 6.2 shows the frequency response of the Active Antenna Preamp and the RF Amp combined. Because the receiver's image frequencies fall within the AM broadcast band, this filter response was chosen to insure that no broadcast band signals would interfere with the DGPS receiver.

The result is overkill, and to save a bit in component cost, two of the six inductors could be eliminated by using 2-pole filters in each section rather than 3-pole filters. To do this, remove the middle inductor-capacitor combination in each circuit and replace with a 1500 pf capacitor. For the RF Amp, replace R4 and R5 with 14k resistors instead of the values shown. Figure 6.3 shows the resulting combined frequency response of the Antenna Preamp followed by the RF Amp, when two coils are used for each rather than three.

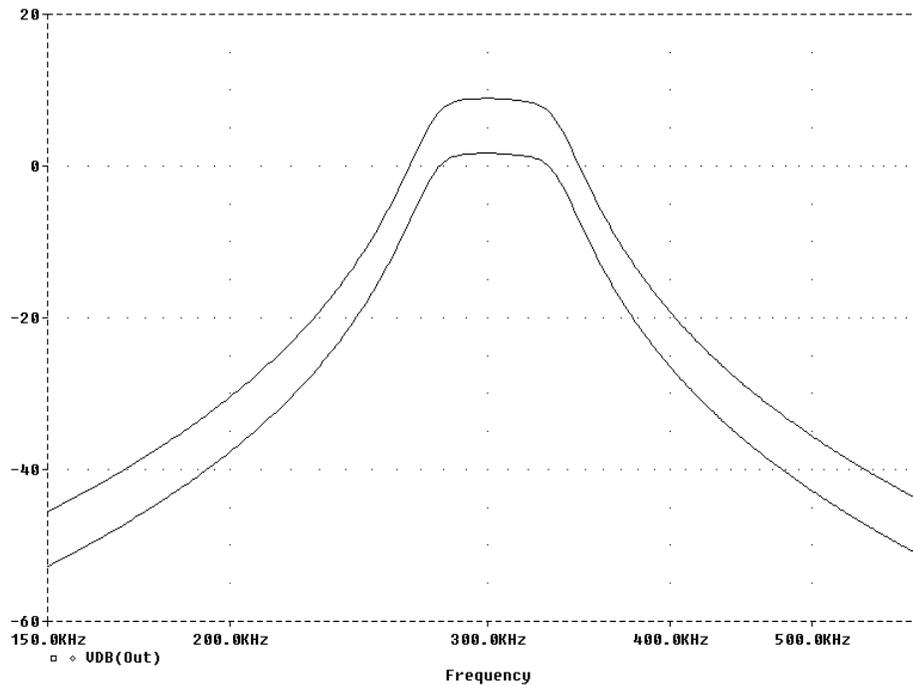


Figure 6.1
RF Amp Frequency Response

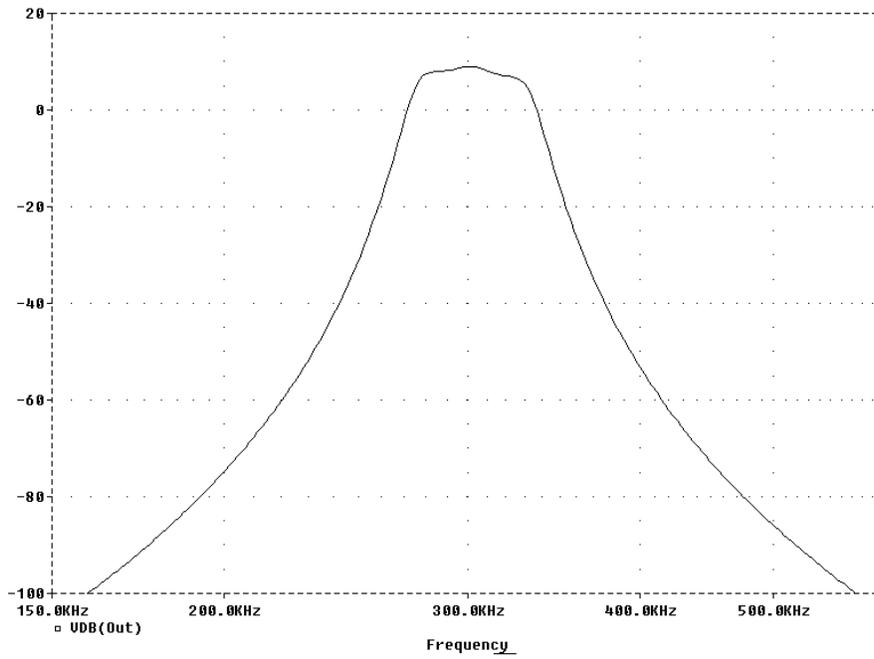


Figure 6.2
Combined Active Antenna Preamp and RF Amp Frequency Response

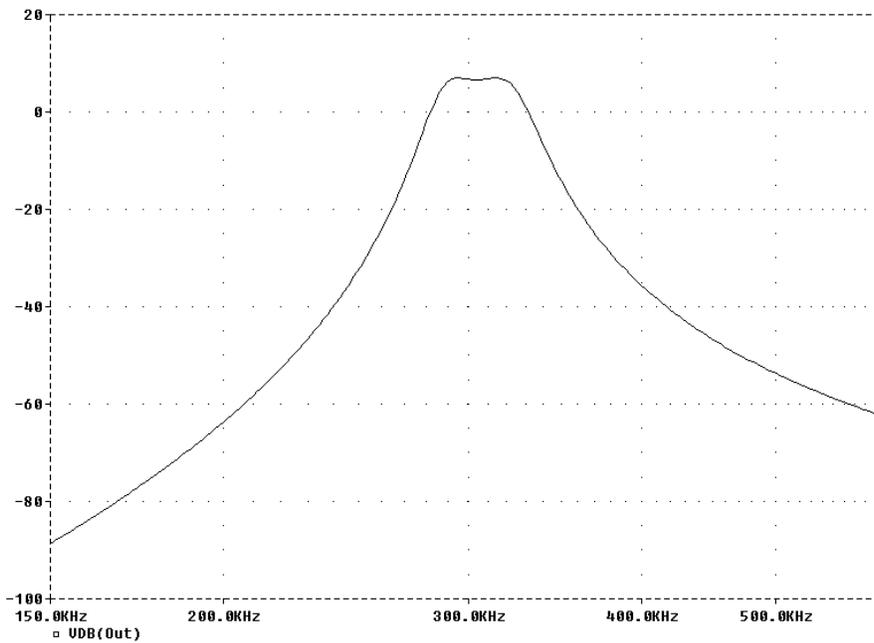


Figure 6.3
Combined Response, Two Coils per Amplifier

7. Receiver

Receiver .wmf contains the schematic for the receiver portion. This is a dual-conversion FM receiver based on a Motorola MC3362 receiver chip. The RF input is applied to the 1st mixer. The other mixer input is the 1st LO (local oscillator), which is on the MC3362 chip, and whose frequency is controlled by L5 and dual varactor diode D1. A frequency synthesizer chip on the Processor schematic phase locks the first local oscillator to the correct frequency, and U3A-U3B form the loop filter for the phase lock loop. Capacitors C12, C13, C15 and C16 provide attenuation of the 1kHz PLL reference frequency. Tuning range for the first LO is 410-450 kHz (ie, 125 kHz above the receiver frequency).

The output of the first mixer is bandpass filtered in the 1st IF Filter, at 122 kHz. Figure 7.1 shows the filter response of this filter, which is easier to tune than the RF filter: basically, just tune the filter for maximum response at 122 kHz. During development, I found that while trying to listen to the DGPS beacon transmitter on Point Loma, CA, at 302 kHz, I had a problem with noise generated by my PC at 300 kHz and about a factor of 20 larger than the beacon I was trying to receive. The design of the first IF filter is the successful result of a long effort to receive the desired signal even in the presence of such a strong, local interfering signal. It is probably more than is needed, and one could eliminate one or two of the filter stages with little impact on performance in most situations.

The first IF filter design uses CMOS inverters as analog gain blocks. Each inverter, if biased to its linear region, has a gain of about -30, and thus these inverters are very useful as very low power, simple gain blocks. You can probably substitute a 74C04 for the MC14069, but do not try to substitute an HCMOS component such as the 74HC04. The gain is much too high and the bandwidth much too large, and they invariably oscillate.

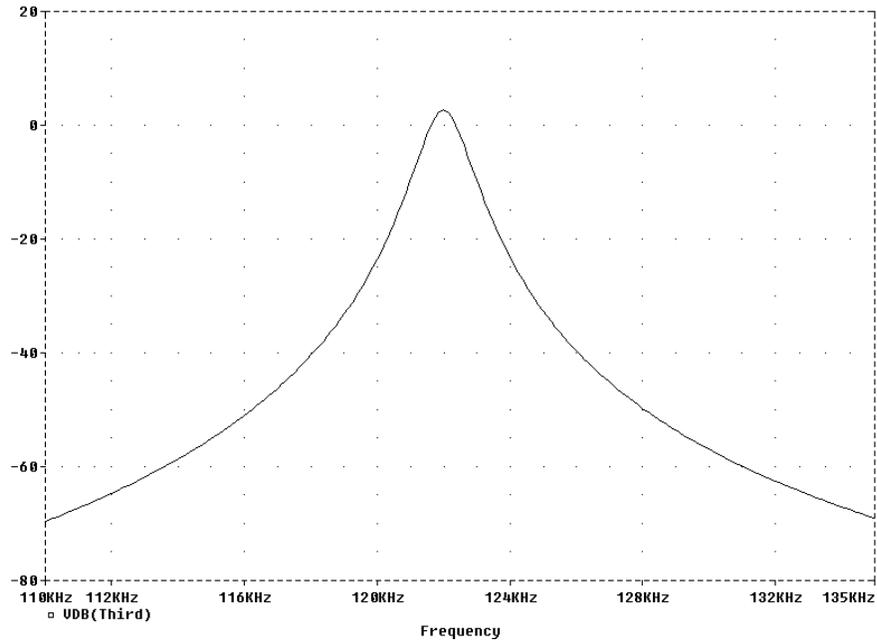


Figure 7.1
1st IF Filter Response

The output of this filter is fed to the second mixer, whose LO input is at 125 kHz, obtained by dividing the 4MHz processor clock. The output is bandpass filtered by an active filter tuned to 3 kHz. The capacitors marked 10 nf in this filter are critical, and capacitors with a tolerance of 2% or better should be used (available from Digikey). The frequency response of the second IF filter is shown on figure 7.2.

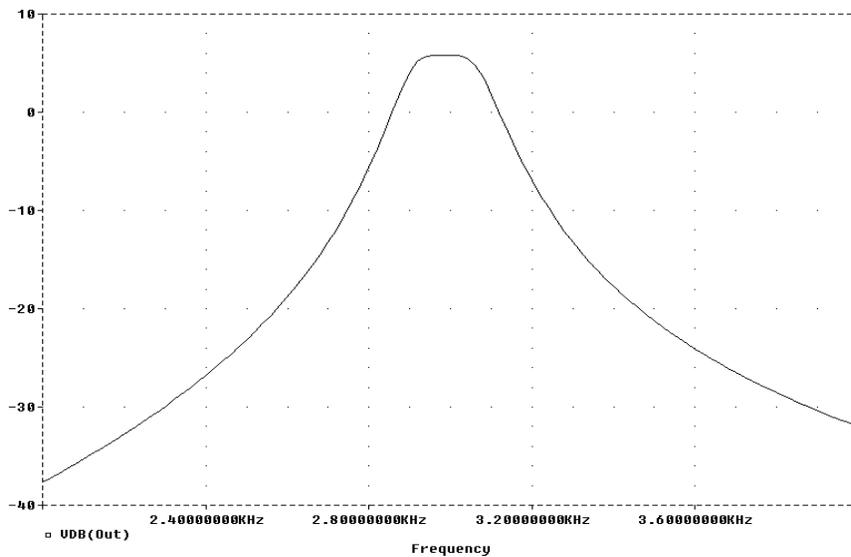


Figure 7.2
2nd IF Filter Response

The output of the second IF filter is fed to a limiter on the MC3362, which amplifies it to a 4v p-p square wave at the Detector Out pin. The MC3362 has circuitry to determine the signal level based on which limiter stage goes into saturation, which is used to determine if an input signal is present or not. Resistor R6 controls the detection threshold -- adjust it so that the receiver shows no input signal when tuned to empty channels, and shows the presence of a signal when tuned to a beacon receiver. The resulting signal CarrDetect is fed to the processor for display on the LCD.

8. PLL Detector

PLL Detector.wmf is the schematic for the FM demodulator. The DGPS signal is a very narrow band FSK signal, with deviation proportional to the bit rate. This circuit accepts the 3khz limited carrier signal from the Receiver, and phase-locks a 3khz oscillator to it. The voltage used to control the PLL oscillator is the demodulated signal. To convert this analog voltage to a digital signal, the top and bottom peaks are found by U5D and U5C respectively. From this, the voltage corresponding to the mid-amplitude point is found (resistors R43-R44) and that is used by U5B operating as a comparator with a small amount of hysteresis. U3C is present simply as a buffer, to provide the data signal to the processor.

At 100 bits per second, the signal at U5A output (pin 1) will be about 1/2 volt peak to peak. At 200 bps it will be about 1 volt, and at 50 bps it will be about 250 mv.

Resistors R41 and R42 limit the charging current for the peak detectors so that the peak is determined by averaging several peaks together, and the discharge resistor (R43 plus R44) sets the decay time constant to tens of bits.

PLL adjustment is accomplished by adjusting R34 so that the VCOout pin on U4 is at 3 khz when the VCOin pin is held at 2.5 volts.

9. Processor

Processor.wmf shows the processor block, which contains the actual processor, the local oscillator synthesizer, and the LCD interface. The processor chosen is a PIC16F84. The processor clock (4 MHz) is generated by an oscillator block on U6, the frequency synthesizer. Jumper W5 allows disconnecting the clock to the processor to allow in-circuit emulation.

Operation is controlled by switches S1 and S2, the UP and DOWN pushbuttons. A single press moves the frequency up or down in 1 kHz steps. The frequency and synchronization/data quality status is displayed on an LCD, which

has two rows of characters, with 16 characters per row. I chose an Optrex 16x2 display with LED backlighting, but any LCD display based on the Hitachi HD44780 controller of size 16x2 or larger would work fine.

There is provision for a third switch in the hardware and software, named MODE. This switch is not implemented in this design.

The first local oscillator for the receiver is controlled by U6, a dual PLL chip of which only one section is used, so a single PLL chip could be used instead. The synthesizer in turn is serially programmed by the processor. See the MC145162 data sheet for more programming information.

The second local oscillator is generated by dividing down the 4MHz crystal oscillator. U6 provides an output which is divided by four, at 1 MHz. This is divided by 8 by U7 to create the 125 kHz second LO.

Jumper W4 allows selection of the output baud rate. At power-up, the processor reads this jumper, and uses that to set the output bit rate at 4800 or 9600 baud. It is read only at power up, so to change baud rates, it is necessary to power down and back up, or press Reset.

To provide parallel data to the LCD, PORTB on the processor does double duty. It is configured as an input port to listen to the receiver status and switches, and then turned into an output port to drive data to the LCD. Because the LCD has internal pullup resistors, it was necessary to add U8 so that the LCD data would be received by a high-impedance circuit. If a processor such as the PIC 16C63 is used instead with more I/O pins, U8 can be eliminated, as well as many of the resistors on the schematic near U9.

A typical LCD display when the receiver is locked is shown below:

302k	ID	SICBWFP
102b	262	+++++++

302k designates the receiver frequency as 302 kHz

100b indicates the input signal is at 100 bits per second

ID is a label for Station ID, which appears below it
(262 is the Station ID for Point Loma, CA)

S..P Labels:

S:	Synthesizer Lock Status.	+:Synth is locked
I:	Input signal detected	+:Signal detected
C:	Carrier Lock	+:FM Demod is locked
B:	Bit Sync	+:Processor is in bit sync
W:	Word Sync	+:Processor is in word sync

small magnet wire, like 32 or 34 guage wire. Now you need to find a capacitor to place across the loopstick to form a resonant circuit. Start with any value, like 100 pf. Get an oscillator, and take the output into a loop of wire near your loopstick, and tune the oscillator to find the frequency of maximum output from the loopstick. If this is above the desired frequency, add capacitance until the desired frequency is achieved. If below, reduce capacitance or remove turns of wire to achieve the desired result. Once you get within the marine beacon band, final tuning should be done with the antenna in its final physical configuration, and wired to the receiver, so that receiver input capacitance is being accounted for.

12. Comments on Design Modifications

A few variations on the design have already been mentioned above, such as reducing the number of inductors in the front-end amplifiers or in the first IF filter.

Below are some further comments on modifications:

Processor: If you use one of the 28- or 40-pin PIC processors, the extra I/O pins would allow the LCD data to be driven from a dedicated port, eliminating U8. Also eliminated would be most of the resistors near the processors which are there to provide for multiplexing of the use of PORTB. If a 16C73 were chosen, the built-in A/D converters would allow measurement of the maximum and minimum values of the input data (top of C31 and top of C32) -- the difference tells you the FM signal amplitude and hence the bit rate. This would be a good way to determine bit rate, rather than the hunting process used by the current design in software.

Also, a larger PIC with a UART would allow a NMEA control signal to be received from the GPS receiver, so that the GPS could control the frequency of the DGPS receiver. Finally, a larger PIC with more program memory would allow implementation of the MODE switch, so that the receiver could, for instance, automatically hunt for a beacon transmission.

For the very experienced builder, a much better and cheaper first IF amplifier can be built. If the first IF frequency is moved to 200 khz, then 200 khz ceramic resonators can be used as filter elements. These resonators have very high Q, and must be individually adjusted with a shunt capacitor. I found the resonators from Digikey could be tuned with 300-400 pf of capacitance. Thus, a filter at the first IF frequency could be built with sufficient selectivity to eliminate the need for the second IF filter. However, such a design would be very difficult to duplicate, which is why I chose conventional tuned circuits for this design.

A similar approach would be to move the first IF frequency very high, like to 6 MHz, and design a crystal filter for the first IF. In that case, the RF Amp and Active Antenna Preamp designs get simpler because the image frequencies are no

longer near the AM broadcast band, and the second IF filter becomes just a single pole lowpass filter. Again: better and cheaper, but very hard for the inexperienced builder to duplicate.

13. Comments on Parts Cost and Selection

The file PartsList.xls is an Excel spreadsheet with detailed parts information, including order numbers and single-quantity prices. Note: I make no claim as to the accuracy of this list!

If you have a well-stocked junk box, you can of course save a fair amount of the project cost, especially for resistors and capacitors. I have called out 1% resistors for the project, but most can be 5%, or even some nearby value.

The LCD in PartsList has LED backlighting. If you shop around, and drop the backlighting, you can generally find a 16x2 LCD character display for about \$6-\$7.

I included the cost of front panel switches in the cost estimate -- in my experience these can be purchased for much less money from a local electronics surplus outlet, like Gateway or others.

14. Initial Debugging and Tuning

This section describes a sequence for initially checking out your receiver after you have built it.

1. With no ICs installed, verify that the voltage regulators are producing +5v and +8v
2. Install U2, and verify that this active filter has the correct frequency response and gain
3. Install U3, and tune the IF filter for max output at 122khz. Verify the gain to be about 1.
4. Tune the RF Amp to achieve the correct frequency response.
5. Install U4, and with 2.5 volts applied to pin 9, adjust R34 so that pin4 (VCOout) is at 3 KHz
6. Install U1. Apply 2.5 volts to pin 23, and adjust L5 so the 1st LO Out pin (pin 20) is at about 430 khz, corresponding to a channel frequency of 308 khz.
7. Install U6. Verify that the crystal oscillator is operating, at 4 MHz.
8. Install U5, U7, U9, U8, and connect the front panel.
9. Verify that the LCD comes up, and that the up and down pushbuttons move the LCD display up and down in 1 khz steps.

10. Observe that there are pulses, spaced 1 millisecond apart, at U6 pin 13. (Indicates the LO Synthesizer is working properly). Press UP and DOWN to move the frequency around, and observe that the LO 1 frequency is correct (122 khz above the displayed frequency).
11. Observe that U7 pin 9 is a 125 khz square wave.
12. Observe that U3 Pin 2 has very little noise, and moves up and down with switch presses in small steps.
13. At this point, the receiver should be working. Connect an antenna to the receiver. If you are in a metal building, tape a wire to a window. You should be able to tune the receiver to your local beacon transmitter, and the LCD display should in short order stabilize on the bit rate display, achieve bit sync and word sync, then show good parity, and finally after 5-10 seconds show frame sync. A few seconds after that, the station ID should appear on the display (sometimes this process can take a long time, up to minutes, depending on signal quality).
14. Adjust R6 so that the incoming signal indicator ('I' on the LCD shows a minus on frequencies with no signal, and a '+' for frequencies with a signal. Note: there may be noise present which causes a signal indication on some 'empty' channels -- this is unavoidable.
15. Verify that there is serial data at the SC104 output which your GPS receiver can read. Note that this output is generated irrespective of the receivers notion about being in sync, so your GPS receiver may determine the station ID well ahead of this receiver.